

LTS. 2225

Date to

P. 2225 2225

## Features

- Compatible with MCS-51™ Products
- 2 Kbytes of Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
  - Data Retention: 10 Years
- 2.7 V to 6 V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Two-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 15 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Five Interrupt Sources
- Programmable Serial Channel
- Direct LED Drive Outputs
- On-Chip Analog Comparator
- Low Power Idle and Power Down Modes

## Description

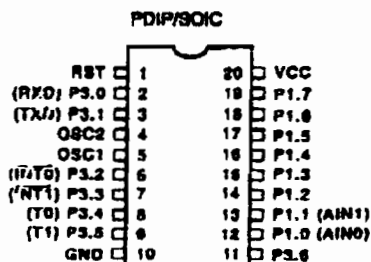
The AT89C251 is a low-power, high-performance CMOS 8-bit microcomputer with 2 Kbytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C251 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89C251 provides the following standard features: 2 Kbytes of Flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five source two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C251 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing it : RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

low cost ( \$3.00 ) 8051

low pin count

## Pin Configuration

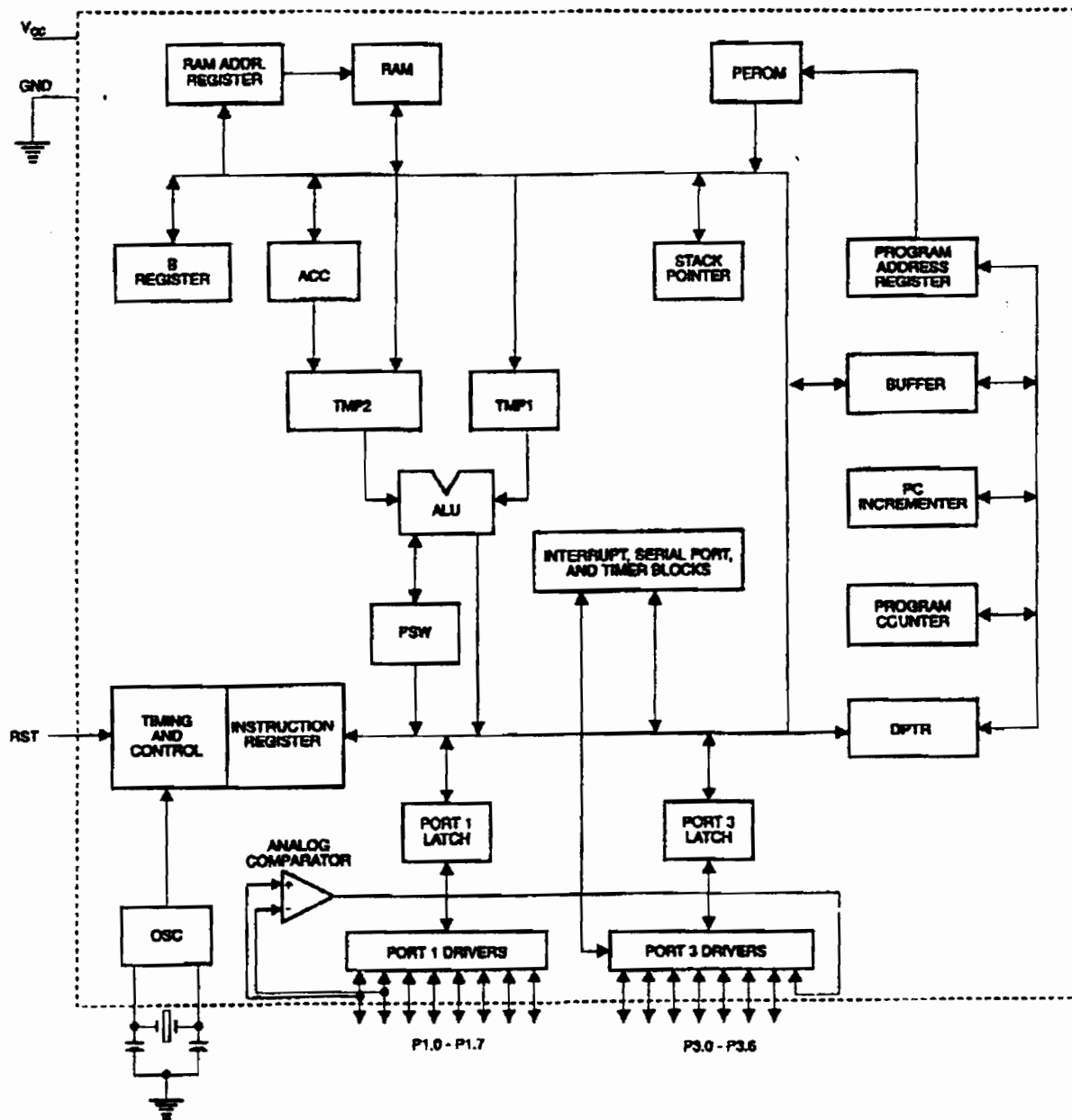


## 8-Bit Microcontroller with 2 Kbytes Flash

## AT89C251 Preliminary



## Block Diagram



## Pin Description

**Vcc**

Supply voltage.

**GND**

Ground.

**Port 1**

Port 1 is an 8-bit bidirectional I/O port. Port pins P1.2 to P1.7 provide internal pullups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (IIL) because of the internal pullups.

Port 1 also receives code data during Flash programming and program verification.

**Port 3**

Port 3 pins P3.0 to P3.6 are seven bidirectional I/O pins with internal pullups. P3.7 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C251 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)

Port 3 also receives some control signals for Flash programming and programming verification.

**RST**

Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device.

**XTAL1**

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

**XTAL2**

Output from the inverting oscillator amplifier.

## Program Memory Lock Bits

On the chip are two lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

### Lock Bit Protection Modes

Program Lock Bits			Protection Type
	LB1	LB2	
1	U	U	No program lock features.
2	P	U	Further programming of the Flash is disabled.
3	P	P	Same as mode 2, also verify is disabled.

## Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

## Idle Mode

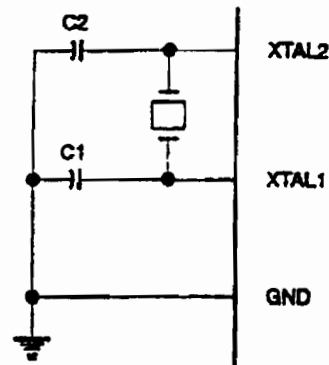
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle is terminated by reset, the instruction following the one that invokes idle should not be one that writes to a port pin or to external memory.

## Power Down Mode

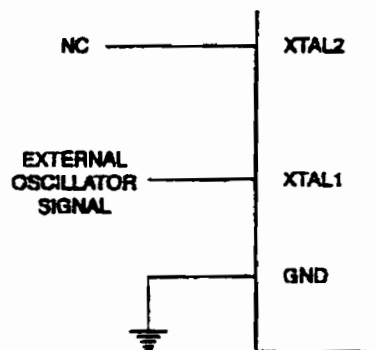
In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V<sub>CC</sub> is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 1. Oscillator Connections



Notes: C1, C2 = 30 pF ± 10 pF for Crystals  
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration





## Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	2.7 V to 6.0 V	AT89C251-12PC AT89C251-12SC	20P3 20S	Commercial (0°C to 70°C)
		AT89C251-12PI AT89C251-12SI	20P3 20S	Industrial (-40°C to 85°C)
		AT89C251-12PA AT89C251-12SA	20P3 20S	Automotive (-40°C to 125°C)
16	3.0 V to 6.0 V	AT89C251-16PC AT89C251-16SC	20P3 20S	Commercial (0°C to 70°C)
		AT89C251-16PI AT89C251-16SI	20P3 20S	Industrial (-40°C to 85°C)
		AT89C251-16PA AT89C251-16SA	20P3 20S	Automotive (-40°C to 125°C)
20	3.3 V to 6.0 V	AT89C251-20PC AT89C251-20SC	20P3 20S	Commercial (0°C to 70°C)
		AT89C251-20PI AT89C251-20SI	20P3 20S	Industrial (-40°C to 85°C)
24	3.3 V to 6.0 V	AT89C251-24PC AT89C251-24SC	20P3 20S	Commercial (0°C to 70°C)

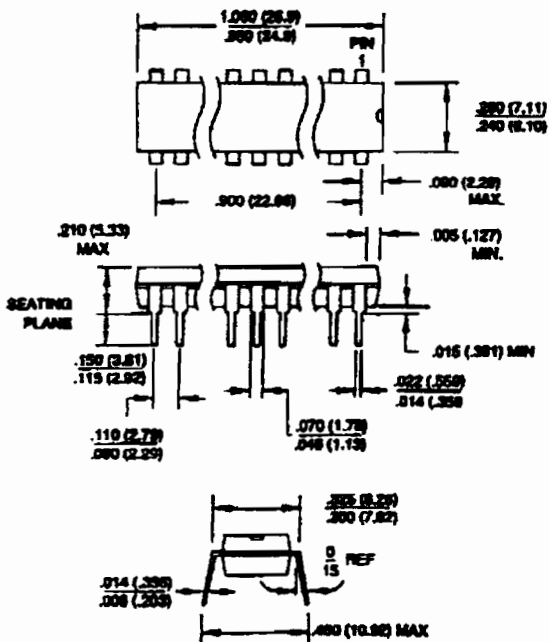
## Ordering Information

Package Type	
20P3	20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

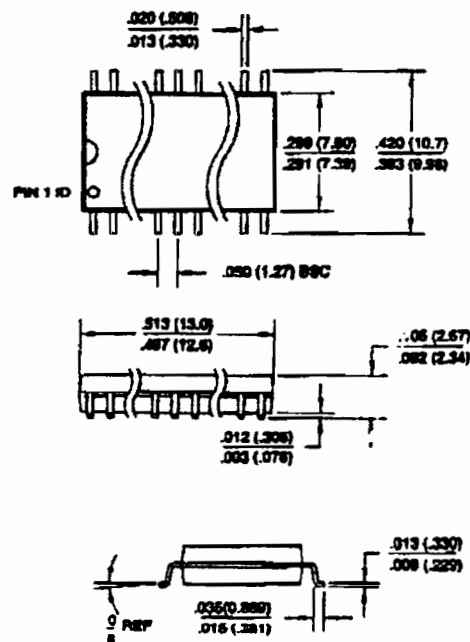
AS-20-20-01S-3 \$79.

## Packaging Information

20P3, 20 Lead, 0.300" Wide,  
Plastic Dual Inline Package (PDIP)  
Dimensions in Inches and (Millimeters)



20S, 20 Lead, 0.300" Wide, Plastic Gull Wing Small  
Outline (SOIC)  
Dimensions in Inches and (Millimeters)



## Absolute Maximum Ratings\*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-1.0 V to +7.0 V
Maximum Operating Voltage .....	6.6 V
DC Output Current.....	25.0 mA

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. Characteristics

T<sub>A</sub> = -40°C to 85°C, V<sub>CC</sub> = 2.7 V to 6.0 V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V <sub>IL</sub>	Input Low Voltage		-0.5	0.2 V <sub>CC</sub> -0.1	V
V <sub>IH</sub>	Input High Voltage	(Except XTAL1, RST)	0.2 V <sub>CC</sub> +0.9	V <sub>CC</sub> +0.5	V
V <sub>IH1</sub>	Input High Voltage	(XTAL1, RST)	0.7 V <sub>CC</sub>	V <sub>CC</sub> +0.5	V
V <sub>OL</sub>	Output Low Voltage <sup>(1)</sup> (Ports 1, 3)	I <sub>OL</sub> = 20 mA, V <sub>CC</sub> = 5 V I <sub>OL</sub> = 10 mA, V <sub>CC</sub> = 2.7 V		0.45	V
V <sub>OH</sub>	Output High Voltage (Ports 1, 3)	I <sub>OH</sub> = -80 µA, V <sub>CC</sub> = 5 V ± 10%	2.4		V
		I <sub>OH</sub> = -30 µA	0.75 V <sub>CC</sub>		V
		I <sub>OH</sub> = -12 µA	0.9 V <sub>CC</sub>		V
I <sub>IL</sub>	Logical 0 Input Current (Ports 1, 2, 3)	V <sub>IN</sub> = 0.45 V		-50	µA
I <sub>TL</sub>	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V <sub>IN</sub> = 2 V		-750	µA
I <sub>IU</sub>	Input Leakage Current (Port P1.0, P1.1)	0 < V <sub>IN</sub> < V <sub>CC</sub>		±10	µA
V <sub>OS</sub>	Comparator Input Offset Voltage	V <sub>CC</sub> = 5 V		20	mV
V <sub>CM</sub>	Comparator Input Common Mode Voltage		0	V <sub>CC</sub>	V
RRST	Reset Pulldown Resistor		40	200	KΩ
C <sub>IO</sub>	Pin Capacitance	Test Freq. = 1 MHz, T <sub>A</sub> = 25°C		10	pF
I <sub>CC</sub>	Power Supply Current	Active Mode, 12 MHz, V <sub>CC</sub> = 6 V/3 V		20/5.5	mA
		Idle Mode, 12 MHz, V <sub>CC</sub> = 6 V/3 V		5/1	mA
	Power Down Mode <sup>(2)</sup>	V <sub>CC</sub> = 6 V		100	µA
		V <sub>CC</sub> = 3 V		20	µA

Notes: 1. Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows:

Maximum I<sub>OL</sub> per port pin: 20 mA

Maximum total I<sub>OL</sub> for all output pins: 80 mA

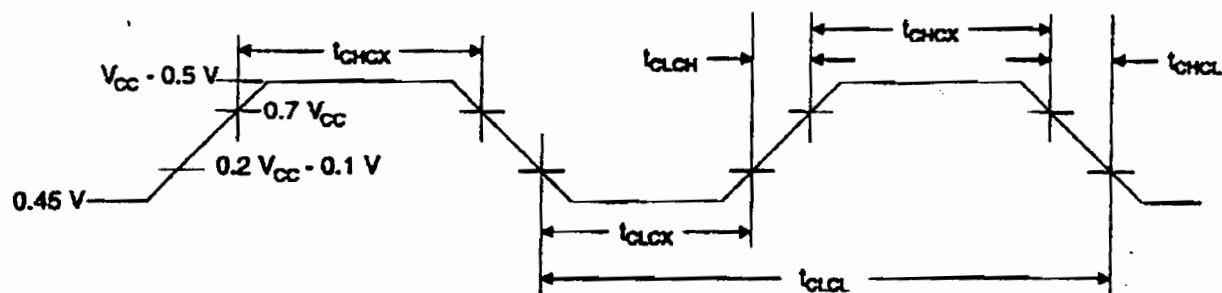
If I<sub>OL</sub> exceeds the test condition, V<sub>OL</sub> may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V<sub>CC</sub> for Power Down is 2 V.





## External Clock Drive Waveforms



## External Clock Drive

Symbol	Parameter	Min	Max	Units
1/t <sub>CLCL</sub>	Oscillator Frequency	0	24	MHz
t <sub>CLCL</sub>	Clock Period	41.6		ns
t <sub>CHCX</sub>	High Time	15		ns
t <sub>CLCX</sub>	Low Time	15		ns
t <sub>CLCH</sub>	Rise Time		20	ns
t <sub>CHCL</sub>	Fall Time		20	ns

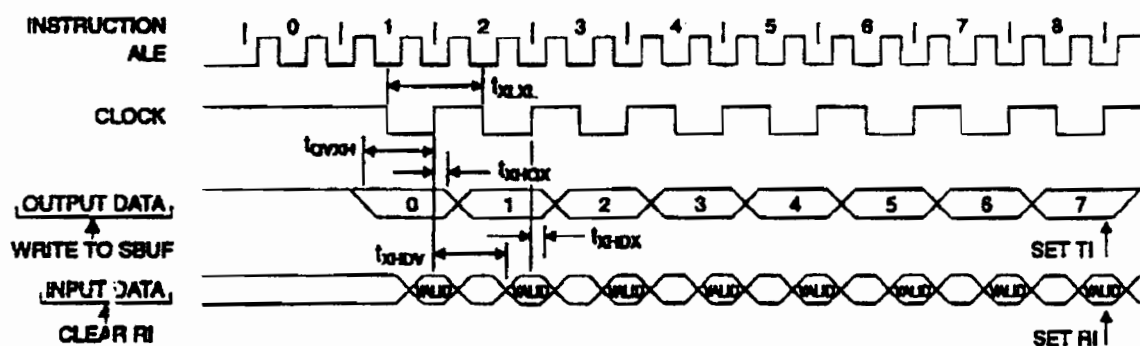


## Serial Port Timing: Shift Register Mode Test Conditions

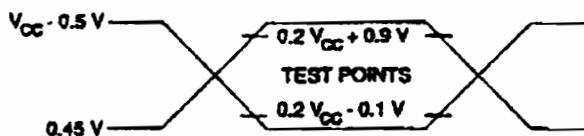
( $V_{CC} = 5.0 \text{ V} \pm 20\%$ ; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
$t_{CLK}$	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		$\mu\text{s}$
$t_{OV2H}$	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}-133$		ns
$t_{OH2X}$	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}-33$		ns
$t_{HD2X}$	Input Data Hold After Clock Rising Edge	0		0		ns
$t_{OH2V}$	Clock Rising Edge to Input Data Valid		700	$10t_{CLCL}-133$		ns

## Shift Register Mode Timing Waveforms



## AC Testing Input/Output Waveforms<sup>(1)</sup>



Note: 1. AC Inputs during testing are driven at  $V_{CC} - 0.5 \text{ V}$  for a logic 1 and  $0.45 \text{ V}$  for a logic 0. Timing measurements are made at  $V_{IH, min.}$  for a logic 1 and  $V_{IL, max.}$  for a logic 0.

## Float Waveforms<sup>(1)</sup>



Note: 1. For timing purposes, a port pin is no longer floating when a  $100 \text{ mV}$  change from load voltage occurs. A port pin begins to float when a  $100 \text{ mV}$  change from the loaded  $V_{OH}/V_{OL}$  level occurs.



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